17, 1999 (now USP 6,154,412); which is a continuation of Serial No. 09/016,300, filed January 30, 1998 (now USP 5,991,221), the entire disclosures of which are hereby incorporated by reference.

IN THE CLAIMS:

Please **cancel** claims 1-22 without prejudice or disclaimer of the subject matter contained therein.

Please **add** new claims 23-27 as follows:

23. A microprocessor on a semiconductor substrate comprising:

a central processing unit;

a flash memory array including:

a first region to be stored therein with a program for the central processing unit, and

a second region to be stored therein with information,

wherein the first and the second region each include electrically erasable and programmable non-volatile memory elements each of which has a layer to store electrons;

a volatile memory circuit capable of storing the information therein; and

a peripheral circuit of the flash memory array coupled to the volatile memory circuit,

wherein the information is transferred from second region to the volatile memory circuit in response to an initialization operation of the microprocessor, and then the peripheral circuit is controlled by the information stored in the volatile memory circuit.

24. A microprocessor according to claim 23, wherein the initialization operation includes a reset operation of the semiconductor integrated circuit.

25. A microprocessor according to claim 23, wherein the electrically erasable and programmable non-volatile memory elements each includes a control gate.

26. A microprocessor according to claim 25, wherein the electrically erasable and programmable non-volatile memory elements each include a floating gate as the layer to store electrons.

27. A microprocessor according to claim 23, wherein said information comprises trimming data.